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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,147	09/15/2003	Christopher E. Warren	12500CON	2147

24116 7590 08/03/2004

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,147	WARREN ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,9-27,63 and 64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,9-27,63 and 64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to application filed on 15 September 2003.

Claims 1-2, 4-5, 9-27 and 63-64 are pending.

The present application is a Continuation of Application 09/643,395 filed 22 August 2000, now abandoned.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "Hardware Extraction Layer 230" (see page 7, line 27; Figures 2a-c).

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- Page 2, lines 4 and 20, "Cantatore" is misspelled.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 64 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 64 recites the limitation "said information" (see line 9). There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 5, 10, 11, 14-17, 21-23, and 63 are rejected under 35 U.S.C. 102(e) as being anticipated by Cantatore et al. [US 5,953,681].

Regarding claim 1, Cantatore et al. discloses a node (see Abstract) for providing a common interface (see col. 2, line 9) for a plurality of system devices (see Abstract, col. 2, lines 2-9). The node disclosed in the reference includes user-configurable software (see col. 43, lines 44-47) for providing a software interface for the system devices (see col. 2, line 9; col. 1, line 65; col. 41, lines 2-5). It is also disclosed user-configurable (see col. 43, lines 44-47) software. This user-configurable software provides a software interface for the system devices as well as multifunctional hardware that provides hardware interface (see col. 75, line 21).

Regarding claim 2, Cantatore et al. discloses an analog system device connected to the node (see col. 78, lines 34-37).

As for claim 5, the node disclosed by Cantatore et al. teaches a processing unit (see col. 2, line 42; col. 75, lines 44-45) connected to the node (see Fig. 24) for processing information received from the system devices and sending information to them (see Fig. 24, col. 75, lines 44-53). The cited reference does teach a network to connect the processing unit for sending and receiving information (see col. 75, lines 20-21).

Regarding claim 10, the network included in the node system disclosed by Cantatore et al. is a Controller Area Network (see col. 2, line 9).

Regarding claim 11, the network included in the node system disclosed by Cantatore et al. is compatible with the node and system devices (see col. 2, line 9).

Regarding claim 14, the node disclosed by Cantatore et al. includes multifunctional hardware (see Abstract). It also includes memory (see col. 75, line 45) that stores software configured by the user (see col. 43, lines 44-47). A microprocessing subunit is disclosed (see col. 1, line 65) that controls (see col. 75, line 22) the operation of the hardware as commanded by the user-configurable software. Cantatore et al. also teaches a plurality of inputs and outputs (see col. 75, line 60) in communication with the microprocessing unit (see col. 75, line 59) for connecting to system devices. A power supply is also disclosed in the cited prior art (see col. 3, line 29; col. 78, line 34).

As for claim 15, the cited prior art teaches a non-volatile memory (see col. 41, line 61) and a volatile memory (see col. 58, line 16).

As for claim 16, Cantatore et al. teaches a microprocessor chip as part of the microprocessing unit (see col. 57, line 20).

Regarding claim 17, Cantatore et al. discloses a bus interface in communication with the memory (see col. 75, line 21). As it is well known in the art all buses have two components: data and address.

Regarding claim 21, the microprocessing subunit disclosed by Cantatore et al. includes a network interface in communication with a network connector (see col. 75, lines 23-24).

Regarding claim 22, an analog to digital converter is disclosed in communication with an analog to digital and digital I/O interface connector (see col. 75, lines 44-46, 58-60).

Regarding claim 23, Cantatore et al. discloses the microprocessing subunit as having a time processing unit (see col. 75, lines 27, 29-31, 35-36) in communication with a switch array in communication with a digital I/O and serial interface connector (see col. 75, lines 64-65).

Regarding claim 63, Cantatore et al. teaches a system for automated control of system devices (see col. 75, line 22). The system in the reference includes a node (see col. 75, line 19) that provides a common interface for the system devices (see col. 75, lines 21-22). It is also disclosed user-configurable (see col. 43, lines 44-47) software that provides a software interface for the system devices as well as multifunctional hardware that provides hardware interface (see col. 75, line 21). The system includes multiple analog and digital system devices (see col. 75, lines 59-62; col. 78, lines 34-37) and a processing unit for communicating and controlling the devices (see col. 2, line 42; col. 75, lines 44-45, 20-21).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4, 9, 13, 20, 24-27 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cantatore et al. [US 5,953,681].

As for claim 4, Cantatore et al. does not disclose the standardization to a single communication protocol. However, the node system disclosed in the reference teaches switching functionality (see col. 57, lines 17-19) and uses a single protocol for electronic communication with the system devices (see Fig. 24; col. 57, lines30, 54-56). Therefore, it is obvious that the communication protocol is standardized to a single protocol (see col. 57, line 29) and that the switching functionality is provided by the node system.

Regarding claim 9, Cantatore et al. teaches analog and digital devices (see col. 51, lines 40-43; col. 78, lines 34-37). Official notice is taken that it is well known in the art for a prior art system to use various types of devices including digital devices and/or serial devices in combination with analog devices.

Regarding claim 13, Cantatore et al. does not expressly include user-configurable software having an application manager, application modules layer or hardware abstraction layer. Nonetheless, the cited prior art does teach managing applications (see col. 57, lines 57-60) via a protocol. As it is well known in the art, a layer, in terms of communication, is a protocol that has the capability of interacting with other routines to provide a required transmission. Cantatore et al. does disclose a protocol for facilitating multiprocessing (see col. 57, line 59), resource allocation (col. 57, lines 15-17), memory management (see col. 58, lines 1-3), and cooperation among independent application modules (see col. 60, lines 43-45). Cantatore et al. does not expressly teach application modules layer for application-dependent system I/O processing. However, the reference does disclose a protocol, which acts depending on the application for the processing of system inputs and outputs (see col. 57, lines 58-59; col. 58, lines 7-9). As it is well known in the art, a module handles specific task within a larger system. Cantatore et al. does not explicitly teach a hardware abstraction layer to consolidate all hardware interfaces accessible from application modules. Nonetheless, it is well know in the art that an abstraction layer provides a common interface between control programs and applications. Accordingly, Cantatore, et al. does provide a common interface between applications (see col. 57, lines 12-13). Therefore, Cantatore et al. does provide a hardware abstraction layer, since it provides a common interface between applications and a control program.

Regarding claim 20, Cantatore et al. does not explicitly includes a background debugging monitor in communication with a background debugging monitor interface connector. Nonetheless, it does disclose a monitoring the state of the node and resetting the microprocessing

unit (see col. 63, lines 51-55). Therefore, it is obvious that a debugging process takes place in the microprocessing unit.

As for claims 24-27, Cantatore et al. teaches analog and digital input and output (see col. 75, lines 59-62). Official notice is taken that it is well known in the art for a prior art system to use various types of I/O including digital I/O and/or serial I/O in combination with analog I/O.

As for claim 64, Cantatore et al. discloses a communication method including connecting system devices to a multifunctional network interface node (see col. 75, lines 19-20). The cited method includes user-configurable software interface (see col. 43, lines 44-47) and a hardware interface (see col. 75, line 21). The reference does not expressly teach standardizing the voltage output levels of the system devices. However, the cited reference provides a power supply that outputs -12/+12V, 0-5V, and -15/+15V (see col. 42, lines 32-37, 42-48). It is obvious that these power supplies would drive the cited system devices to output the voltages mentioned above. Cantatore et al. does not expressly disclose the standardization to a single communication protocol. However, the node system disclosed in the reference uses a single protocol for electronic communication with the system devices (see Fig. 24; col. 57, lines 30, 54-56). Therefore, it is obvious that the communication protocol is standardized to a single protocol (see col. 57, line 29). The cited prior art teaches connecting the node to a processing unit where this unit receives and processes information and commands from the system devices (see col. 2, line 42; col. 75, lines 44-53).

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cantatore et al. [US 5,953,681] in view of Collins [US 5,671,355].

Regarding claim 12, Cantatore et al. does not disclose expandable and updateable user-configurable software. However, Collins teaches software that is configurable/reconfigurable across a network (see col. 3, lines 63-67; col. 4, lines 1-5). It is obvious that reconfiguring software would include expanding and updating. In order to expand the control of the circuitry disclosed by Cantatore et al., it would have been obvious to modify the user-configurable software disclosed.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cantatore et al. [US 5,953,681] in view of Bolles et al. [US 4,970,466].

Regarding claim 18, Cantatore et al. teaches a microprocessing unit (see col. 69, line 20; col. 75, lines 59-60) including a port for asynchronous communication (see col. 69, lines 20-28) in communication with a high-speed serial interface connector (see col. 41, line 2). Although the cited prior art does not explicitly recites an asynchronous serial port or a serial device transceiver, it does disclose a port that uses a common standard for asynchronous serial transmission (see col. 41, line 2). Accordingly, Bolles et al. teaches the use of a microprocessing subunit having an asynchronous serial port in communication with a high-speed serial interface connector (see col. 5, lines 5-13). As one of ordinary skill in the art knows, a serial port is used for connection of serial devices, such as a modem or mouse.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cantatore et al. [US 5,953,681] in view of Dunn et al. [US 5,349,640].

Regarding claim 19, Cantatore et al. discloses a microprocessing unit including a serial port in communication with a serial port interface connector (see col. 64, lines 21-23, 38-39). However, Cantatore et al. does not explicitly teach this microprocessing unit for synchronous communication. However, Dunn et al. teaches the use of synchronous serial communication (see col. 12, lines 55-61). It would have been obvious to combine the node disclosed by Cantatore et al. with the Dunn et al. disclosure in order to implement a high speed serial data bus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 9:30-6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

alc
July 27, 2004

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